

Docket No. 249114US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Takashi OHSAWA

SERIAL NO: NEW APPLICATION

GAU:

FILED: HEREWITH

EXAMINER:

FOR: SEMICONDUCTOR INTEGRATED CIRCUIT DEVICE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- ☒ The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- ☐ Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- ☐ A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

- ☐ Each item of information contained in this information disclosure statement was first cited in any communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- ☐ No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- ☒ Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

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DOCKET NO.: 249114US2/dlb

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STATEMENT OF RELEVANCY

Reference AO (2002-246571) on Form PTO-1449:

Single transistor DRAM cell on Silicon-on-insulator (SOI) is disclosed whose floating body is used as a charge storage node. A second gate is coupled to the body in order to enhance the signal amount and the retention time.

Form PTO 1449
(Modified)U.S. DEPARTMENT OF COMMERCE
PATENT AND TRADEMARK OFFICEATTY DOCKET NO.
249114US2SERIAL NO.
NEW APPLICATION

LIST OF REFERENCES CITED BY APPLICANT

APPLICANT
Takashi OHSAWAFILING DATE
HEREWITH

GROUP

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA	6,621,725 B2	09/16/03	Takashi OHSAWA			
	AB	6,538,916 B2	03/25/03	Takashi OHSAWA			
	AC	6,617,651 B2	09/09/03	Takashi OHSAWA			
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						
	AM						
	AN						

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION	
					YES	NO
	AO	2002-246571	08/30/02	Japan (with English Abstract)		X
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					

OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)

	AW	Charles KUO, et al., "A Capacitorless Double-Gate DRAM Cell Design for High Density Applications", IEDM TECH. DIGEST, Dec. 2002, pgs. 843-846
	AX	
	AY	
	AZ	<input type="checkbox"/> Additional References sheet(s) attached

Examiner

Date Considered

*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.